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Protecting a Device Against Unintended Use in a Secure Environment

Field of the Invention

The present invention relates to a method of protecting a device against unintended use in a secure environment and, in particular, in a conditional access environment. The invention also relates to a device for executing applications that involve conditional access to valuable contents and/or valuable services.

Background of the Invention

Examples of applications that involve secure transactions are electronic payment and banking; examples of applications that involve conditional access are Digital Pay TV, recording of Digital TV and Video on Demand. A device for executing such applications can be a module that is embedded in an environment such as a Set-Top-Box, a chip embedded on the motherboard of a Set-Top-Box, a Smart Card reader or a pluggable module such as a PC card that typically includes a Smart Card reader. While hardware components in the module ensure high performance for tasks such as descrambling of real time video streams, the Smart Card mainly has a security functionality. Application code is typically stored into an external memory of the device, such as a FLASH memory.

Conventionally, these devices rely on security that resides in the Smart Card. To the extent, however, that overall security depends on procedures contained in application code stored in external or even in internal memory of the device, the security functions of the Smart Card can be worked-around by replacement or modification of application code.

Summary of the Invention

The present invention provides a secure architecture for a device that executes applications under high requirements of security.

According to a first aspect of the invention, a method of protecting a device against unintended use in a secure environment is provided, where the device is adapted to execute applications that involve secure transactions and/or conditional access to valuable contents and/or services, and the device includes an integrated circuit that has a central processing unit, an internal memory and input/output connections for external memory, all incorporated on a single chip. The external memory and the chip are uniquely linked by encrypting sensitive application code and data with a secret key stored in a secured memory area of the internal memory of the chip, the encrypted code and data being then stored in the external memory. Any use of the sensitive application code and data will be possible only after successful decryption with the secret key. Preferably, a random number and its hash value are also encrypted with the secret key and stored in the external memory. On each reset of the device, the encrypted random number and the hash value are decrypted with the secret key, and decryption of the encrypted sensitive code and data is only allowed if the decrypted hash value equals a hash value calculated from the decrypted random number. As a result, the chip and external memory are uniquely paired, i.e. the chip cannot be used with an external memory the sensitive contents of which have been altered or exchanged.

The invention also provides a device for executing applications that involve secure transactions and/or conditional access to valuable contents and/or services. The device includes an integrated circuit that has a central processing unit, an internal memory and input/output connections for an external memory, all incorporated on a single chip. The internal memory includes a secured memory area accessible to the central processing unit only. The secured memory area contains a secret encryption key used for encryption of sensitive data stored in the

external memory. Preferably, the chip includes a random number generator. A hash value is obtained from a random number generated by the random number generator, the random number with its hash value are encrypted with the secret key, and the encrypted random number with its hash value are and stored in the external memory. As a result, the device has a chip that is uniquely paired with the external memory. Since the sensitive data and/or code are of such nature that proper execution of an application by the device will not be possible unless these data and/or code have been successfully decrypted, and the chip will not decrypt the data and/or code unless it has successfully checked its pairing with the external memory, the device is effectively protected from use with other than authentic contents of the external memory.

The secured memory area may contain authenticity verification data. The internal memory may also include a read only memory area containing mandatory authenticity verification code allowing an application to be executed only after successful verification of authenticity. Therefore, only authentic application code is executed by the device, and any replacement of application code attempting to circumvent safety functionality will not be successful.

As used herein, "authenticity" is understood in a broad sense. In the preferred embodiments of the invention, as defined in the appending claims, "authenticity" includes integrity, and any fraudulent modification of application code or sensitive data results in refusal by the device to execute the application.

In further preferred embodiments of the invention, as defined in the appending claims, any sensitive application code and data are never visible in the clear from outside of the device. Sensitive application code and data are stored in encrypted form and decrypted within the device for execution of the application. By adding confidentiality to authenticity, an attack will be even more difficult, if not impossible, because the contents in memory, as visible from outside of the device, will not be intelligible.

According to a further aspect of the invention, any application code down-loaded into the device is signed with a private key of an asymmetric key pair and proper execution of the application is subject to a verification of the signature with a public key of the key pair. In addition, any application code stored into the external memory is encrypted with a secret key that is stored in a secured memory area of the internal memory.

Further aspects of the invention are the following:

Application code down-loaded into the device is signed with a private key of an asymmetric key pair and proper execution of the application is subject to a verification of the signature with a public key of said key pair.

The signature is generated by obtaining a hash value from said application code and encrypting the hash value with the private key.

The public key of said key pair is stored in an internal read only memory of the device.

The public key of said key pair is stored in an internal secured memory area of the device.

A secure architecture designer's public key is stored in an internal read only memory of the device, a customer's public key is signed with the designer's private key and stored in the external memory, the customer's public key is retrieved by decrypting with the designer's public key read from the read only memory, the encrypted customer's public key read from the external memory, and the signature is verified.

The public key of said key pair is downloaded with the signed application code and a hash value of the public key is encrypted with a private key the corresponding public key of which is stored in internal read only memory of the device, and the encrypted hash value is also downloaded to the device.

The application code is downloaded into the device, encrypted with the secret

A device for executing applications that involve conditional access to at least one of valuable contents and services, including an integrated circuit that has a central processing unit, an internal memory and input/output connections for external memory incorporated on a single chip, characterized in that the internal memory includes a secured memory area accessible to the central processing unit only and containing a secret encryption key used for encryption of sensitive data stored in the external memory. The chip includes a random number generator, and a hash value is obtained from a random number generated by the random number generator, the random number with its hash value are encrypted with said secret key, and the encrypted random number with its hash value are and stored in the external memory.

The encryption is limited to sensitive application code and data.

The external memory is a flash memory.

A secret device key associated with each particular device is stored in said secured memory area, sensitive data are encrypted with said secret device key, the encrypted sensitive data are stored in the external memory and the encrypted sensitive data in the external memory are decrypted and verified at least at each reset of the device.

The secured memory area includes a signature verification public key used for verification of a signature attached to application code to be executed by the device.

Application code to be executed by the device is stored in said external memory with an attached signature and with a signature verification key encrypted with a private key, a corresponding public key being stored in the read only memory of the device.

A encrypted hash value of sensitive application code and data is added to application code stored in said external memory.

The secured memory area includes personalization data pertaining to an

intended use, an intended customer and an intended configuration of the device.

The external memory includes an application code storage into which application code can be loaded subject to compliance with said personalization data.

The secured memory area is loaded with at least one secret key and a hash value of the content of the secured memory area prior to delivery of the chip to a customer.

The chip comprises intrusion detection means for, in response to a detected intrusion, erasing at least essential parts of said secured memory area.

The chip includes a watch-dog and the chip is reset or at least essential parts of said secured memory area are erased when no activity is detected by the watch-dog within a predetermined time.

The chip includes a clock monitor and any abnormal variation of the chip clock rate causes the chip to reset or at least essential parts of said secured memory area to be erased.

The chip has outer connection terminals that are variably assigned to internal connections, and a secret terminal assignment is used to supply secret keys and/or procedures to said memory.

The device comprises a read only memory area that contains mandatory authenticity verification code allowing an application to be executed by the device only after successful verification of authenticity, the secret memory area also containing authenticity verification data, and wherein said authenticity verification code is contained in a boot procedure. The internal memory includes a ROM and at least part of said authenticity verification data is obtained by applying a predetermined hash function to at least a predefined part of the ROM content. The authenticity verification code applies said predetermined hash function to said predefined part of the ROM content and compares the hash value with a corresponding part of the authenticity verification data.

At least part of said authenticity verification data is obtained by applying a predetermined hash function to the content of the secured memory area. The authenticity verification code applies said predetermined hash function to the content of the secured memory area and compares the hash value with the corresponding part of the authenticity verification data.

Short Description of Drawings

Further advantages and features of the invention will become apparent from the following description with reference to the appending drawings. In the drawings:

Fig. 1 is an overall schematic diagram of a device with a generic secure system architecture for a Conditional Access Module (CAM) and a Smart Card Reader (SCR);

Fig. 2A and 2B are diagrams illustrating different embodiments of procedures for preparing signed application code to be down-loaded into the device;

Fig. 3A to 3D are diagrams illustrating corresponding embodiments of signature verification procedures within the device;

Fig. 4A is a block diagram illustrating a procedure for preparing encrypted application code to be downloaded into the device;

Fig. 4B is a flow-chart illustrating decryption of the down-loaded application;

Fig. 5A and 5B are flow charts illustrating encryption and decryption of application code stored in external memory of the device;

Fig. 6 is a diagram illustrating a procedure of chip pairing whereby a chip is uniquely linked to contents in an external memory of the device;

Fig. 7 is a diagram illustrating a chip pairing verification procedure;

Fig. 8 is a diagram illustrating a first step of a chip personalization process; and

Fig. 9 is a diagram illustrating a second step of a chip personalization process;

Fig. 10 is a schematic representation of a variable assignment between external chip pins and internal chip signal lines; and

Fig. 11 is a block diagram of an intrusion detection arrangement.

Detailed Description of Preferred Embodiments

Overall Device Design

Referring now to Fig. 1, the device of the present invention includes an application specific integrated circuit (ASIC) that is generally designated at reference numeral 10. The ASIC 10 incorporates, on a single semiconductor chip, a number of components; among these components, the following are essential to the invention (although the ASIC will typically include other components):

- a microprocessor unit (μP) 12,
- a read only memory (ROM) 14 connected to μP 12,
- an internal secured memory area (ISMA) 16 also connected to μP 12.

Preferably, as shown in Fig. 1, the ASIC also includes a hardware encryption unit 18 connected to μP 12 and to an external random access memory (RAM) 20 via a bi-directional interface 22, symbolized in Fig. 1 by a double arrow. In addition to external RAM 20, the device 10 has an external Flash memory 24 connected to μP 12 via a bi-directional interface 26 symbolized in Fig. 1 by a double arrow. The device 10 further includes a bi-directional interface 28 for connection to an external Smart Card (SC) 30.

In a specific embodiment, the device 10 incorporates conditional access (CA) functionality. Such a device is generally referred to as a CAM (Conditional Access Module) for use with a Set-Top-Box (STB) in a digital TV (DTV) environment. A CAM can be embedded within the STB, or it is a pluggable PC (PCMCIA) card fitting into a Common Interface (CI) slot of the STB, and incorporates a Smart Card Reader (SCR). Other embodiments of the device 10 include a SCR for use with a Personal Computer under high requirements of security.

Signed Down-Load

With reference to Fig. 2A, a first aspect of the invention is that any application to be executed by the device, at least to the extent it involves sensitive transactions, is checked for authenticity and integrity. Generally stated, the application code is signed with a key, and execution of the application by the device is subject to a positive verification of the signature. Various embodiments of this concept are proposed herein.

In each embodiment, a hash function obtains a hash value from the application code. The hash value is encrypted with a private key of a key pair. The public key of the key pair is stored in the memory of the device and, being a public key not specific to a particular customer, it can be stored in ROM 14.

In a first embodiment, as seen in Fig. 2A, the key pair includes a private key referred to as "SignDownPrK"; in the first embodiment, this SignDownPrK is a Secure Architecture Designer's private key (SADPrivateKey). The corresponding public key (SADPublicKey) is stored in ROM 14. In Fig. 2A, "C" is application code in the clear, intended to be downloaded into the device. Further, a signature "D" in Fig. 2A is the hash value of the application code as encrypted with the private key.

With reference to Fig. 3A, where like symbols as in Fig. 2A are used, C and D are received in the device. A hash value C' is obtained from C with a hash function read from ROM 14. D is decrypted to D' with the public key (SADPublicKey) read from ROM 14 using an algorithm stored in ROM 14. If C' equals D', the application code C is valid and enabled for execution by the device; otherwise, the application code C is erased. After validation of application code C, it is loaded into RAM 20, preferably after encryption in RAM encryption interface 18. The microprocessor 12 will have access to application code in RAM 20 without significant loss of performance even though it is encrypted and must be decrypted by RAM encryption interface 18 prior to its execution, the RAM encryption interface being implemented in hardware. Alternatively or in addition, the validated application code is permanently stored, e.g. in external memory 24, but preferably in encrypted form.

In a second embodiment, a customer's private key (CustomerPrivateKey) is used for encryption of the hash value of application code C, rather than SADPrivateKey.

As used herein, "customer" means an organisation that offers valuable services and contents to end-users. Typically, the "customer" would purchase the device of the present invention, or at least the ASIC 10, from the Secured Architecture Designer (SAD) or a contract manufacturer of the SAD, and supply the device to an end-user in a finished product.

Now, in a first variant of this second embodiment, the public part of a customer key pair is stored in internal secured memory area (ISMA) 16. As seen in Fig. 3B, that public key is read from ISMA 16 and used for verification of signature D. All other steps are the same as those in Fig. 3A.

In a second variant of the second embodiment, the Secure Architecture Designer's public key (SADPublicKey) is stored in ROM 14, and the customer's public key is signed with the SAD Private Key and can, therefore, be safely stored

in the external memory 24. With reference to Fig. 3C, the CustomerPublicKey is first retrieved by decrypting, with SADPublicKey read from ROM 14, the encrypted customer's public key read from external memory 24, and then signature D is verified as in Fig. 3B.

In a third variant of the second embodiment, and with reference to Fig. 2B, a protected version of the CustomerPublicKey is down-loaded with the application code C into the device, so that the CustomerPublicKey will never be available in the external memory 24. Specifically, a hash value of CustomerPublic key is encrypted with SADPrivateKey to "F" and downloaded into the device along with CustomerPublicKey "E". With reference to Fig. 3D, verification of the application's signature is preceded by a verification of CustomerPublicKey. Downloaded CustomerPublicKey E is hashed and the hash value E' is compared with the result F' of decrypting, with SADPublicKey, the downloaded encrypted hash value F of CustomerPublicKey. If E' equals F', the verification proceeds to the verification of the application's signature D, as in Fig. 3C; otherwise, the application code C is rejected.

Except for the third variant of the second embodiment of the signed download method, the downloaded application code can be stored in the external memory 24 of the device.

Encrypted Down-Load

While the procedures disclosed so far ensure authenticity and integrity of an application to be executed by the device, a further proposal of the invention is to add confidentiality. As far as downloading of an application is concerned, confidentiality is achieved by encrypting the application code prior to its download.

With reference to Fig. 4, application code to be downloaded into the device is encrypted to "A" with SADSecretKey, a secure architecture designer's symmetric key. A hash value of the application is encrypted to "B" with SADSecretKey. The encrypted application and its encrypted hash value, A and B, are now downloaded into the device. With reference to Fig. 4B, A and B are decrypted to A' ad B', respectively, using SADSecretKey read from the secured memory area 16. A' (the application code in the clear, if correctly decrypted) is hashed to B'', and B'' is compared with B' (the application's code hash value, if correctly decrypted). If B'' equals B', the down-loaded and decrypted application code A' is validated; otherwise, A' is rejected.

The validated application code can now be used, e.g. it can be permanently stored in external memory 24 but, in the preferred embodiment, it will be encrypted before it is stored.

External Memory Encryption

In the scenario depicted in Fig. 5A, application code is available from RAM 20 after a signed and/or encrypted download, for example. Being a validated application, it can be stored in permanent external memory 24, but preferably not in the clear as far as sensitive software code and data are concerned.

Initially, the ASIC thus selects sensitive code and data to be encrypted. Depending on the required level of security and flexibility, an encryption key KF is used directly or a derived key is used. As a first option, KF is the SADSecretKey read from secured memory area 16. The selected sensitive code and data are encrypted with that key and stored in external memory 24, along with other, non-sensitive code and data.

As a second option, KF is the ChipSecretKey, also read from the secured memory area.

As a third option, a random number "RN" is used as the encryption key, KF=RN, RN is encrypted with SADSecretKey read from the secured memory area 16, and the encrypted random number is stored in external memory 24 as "RNEnc".

As a fourth option, the sensitive code and data are compressed by the ASIC prior to encryption.

As a fifth option, a secret chip random number "ChipRandomNumber" is fetched from the secured memory area 16. The ChipRandomNumber and a hash value thereof are encrypted with encryption key KF to X and Y, respectively. The encrypted random number X and its encrypted hash value Y are stored in external memory 24, along with the encrypted sensitive code and data and other, non-sensitive code and data.

As a sixth option, the sensitive code and data are hashed and encrypted with key KF. The result EncH is stored in external memory 24 along with the encrypted sensitive code and data and other, non-sensitive code and data.

With reference now to Fig. 5B, and according to the respective option among options 1 to 6, the appropriate key KF must be determined. With key KF, the encrypted contents of the external memory 24 are decrypted and can be used, e.g. for execution of an application.

If it is option 1, KF is SADSecretKey, as read from the secured memory area 16.

If it is option 2, KF is ChipSecretKey, as read from the secured memory area 16.

If it is option 3, KF is obtained by decrypting the encrypted random number RNEnc read from the external memory 24 with the SADSecretKey read from secured memory area 16.

With option 4, the decrypted contents of external memory 24 are decompressed

before they are used.

Option 5 requires an integrity check for the contents of external memory 24. The encrypted random number X and its encrypted hash value Y are decrypted to X' and Y' with KF, the decrypted random number X' is hashed to Y'' and the result is compared with the decrypted hash value Y'. If Y'' equals Y', the content of external memory 24 is validated; otherwise, it is rejected.

With option 6, integrity of the encrypted sensitive code and data is checked. Specifically, the encrypted hash value EncH is read from external memory 24 and decrypted to H with key KF. A hash value H' is calculated from the decrypted sensitive code and data. Only if both hash values H and H' are equal, the decrypted sensitive code and data are validated.

It is understood that options 4, 5 and 6 are not mutually exclusive and can be used separately or jointly with any of options 1 to 3.

Chip – External Memory Pairing

To further protect the device, the invention proposes to uniquely link the chip of the device with the contents of the external memory 24 (External Memory – ASIC Pairing).

With reference to Fig. 6, sensitive application code and data are identified within external memory 24 and encrypted to "I" with secret chip key "ChipSecretKey" read from the secured memory area 16, and I is stored in external memory 24. The sensitive application code and data are such that proper execution of the application is impossible without successfully decrypting the code and data. The random number generator within the chip of the device generates a random number "RNG" which is hashed to "K". The random number RNG and its hash value K are encrypted to "J" with "ChipSecretKey", and J is also stored in

external memory 24. The chip is now uniquely linked to the external memory 24.

With reference to Fig. 7, the chip verifies its pairing with external memory 24 at least after each reset of the device. Specifically, J (the encrypted random number and its hash value) is read from external memory and decrypted with "ChipSecretKey" to "W" and "Z". The calculated hash value of W, " Z' ", is compared with the decrypted hash value Z of random number W. Only if Z and Z' are equal, pairing is confirmed and the sensitive application code and data can be retrieved from I read from the external memory by decrypting I; otherwise, some appropriate action is taken to prevent unintended use of the device.

Chip Personalization

Immediately after its manufacturing, the chip of the device only has a basic functionality by software and data stored in ROM 14. Software initially stored in ROM 14 includes a boot procedure, a download routine, a cryptography library and other basic functions. Data initially stored in ROM 14 includes a Serial Number, the SADPublicKey and a hash value over the ROM content. The secure memory area 16 will be empty, and the chip will be without defence against unintended use.

Therefore, according to a further proposal of the invention, the chip is personalized before it is delivered to a customer.

With reference to Fig. 8, a first level personalization of the chip includes storing a secret symmetric personalization key "PersoSecretKey" in the secured memory area 16 (ISMA). An internal information field within secured memory area 16, "ISMAInfo", is updated to indicate that PersoSecretKey is available. A hash value ISMAContentHash over the content of the secured memory area 16 is calculated and also stored in the secured memory area.

The chip can now be shipped to a customer where a second level personalization will be made before delivery of the chip to an end-user within a finished product. Alternatively, the second level personalization is already performed by the Secure Architecture Designer (SAD) before the chip is shipped to the customer or end-user.

With reference to Fig. 9, a second level personalization is illustrated which can be performed by the Secure Architecture Designer or by a customer. The Secure Architecture Designer provides a particular personalization application the purpose of which is to write into the device sensitive data and information pertaining to the intended use of the device. For download into the device, the personalization application "PersoAppli" is encrypted with the secret symmetric personalization key "PersoSecretKey", and a hash value of the application code is calculated and signed with a Secure Architecture Designer's private key "SADPrivateKey". Alternatively, both the application code and its hash value signed with "SADPrivateKey" are encrypted with the secret symmetric key "PersoSecretKey" and downloaded into the device. The device will be able to decrypt the encrypted application code with "PersoSecretKey" read from the secured memory area 16, and to check the signature of its hash value with "SADPublicKey" read from ROM 14. After execution of the personalization application by the device, all sensitive data and information have been written into the device, "ISMAInfo" is updated, a new "ISMAContentHash is computed and stored, "PersoSecretKey" is erased and the application is also erased.

Variable Terminal Assignment

As should be clear from the preceding description, the method of the present invention requires access to protected parts of the chip in order to initiate the chip with basic confidential and sensitive data and, in particular, those written into secured memory area 16. In order to protect the chip against non-authorized access to sensitive parts, the invention proposes a secret access channel that must

be used to access sensitive parts of the device.

With reference to Fig. 10, the ASIC includes a silicon core body 30 with a number of internal chip connections 32 and a number of external terminals 34 (pins or pads). Within the package 36 of the ASIC, an internal row of parallel conductor lines 38 permits to connect any of the internal chip connections to any of the external terminals 34. At least some of the assignments between internal chip connections 32 and external terminals 34 are variable and are materialised by selectively operated switches such as switches 40, 42 in Fig. 10. In order to establish a secret access channel, selective ones of the switches 40, 42 are closed and, after use of the secret channel such as for the above personalization steps, can be opened and left open.

Intrusion Detection

Whenever an intrusion of any kind is detected, appropriate steps are taken to prevent unintended use of the device. Typically, the contents of the secured memory area 16 are erased.

With reference to Fig. 11, the ASIC 10 includes an intrusion detector 50. In the proposed embodiment, the secured memory area 16 within ASIC 10 is a RAM that needs a continuous power supply to maintain information stored therein. Secured memory area 16 (RAM) receives power from an external battery 52 connected to external supply and ground terminals of the ASIC. A controllable switch 54 is inserted in the supply path of memory area 16. Switch 54 is normally closed and is controlled by intrusion detector 50. Intrusion detector 50 has a number of inputs connected to corresponding monitoring devices. One such monitor device can be a photo-transistor 56 that would detect any light penetrating into the chip package upon physical attack of its envelope. Another monitor device can be a temperature sensor 58 that would detect any abnormal temperature. The intrusion detector 50 is also connected to the main device power supply and to ground and would detect any abnormal supply voltage or power

consumption. Yet another input to intrusion detector 50 is connected to the system clock generator 60 and would detect any abnormal clock rate. A watch-dog 62 connected to a further input of intrusion detector 50 would detect any abnormal absence of activity from microprocessor 12 within a given time. Any failure of an integrity, authenticity or signature check is also signalled from microprocessor 12 to the intrusion detector 50.

Each abnormal condition signalled to the intrusion detector 50 by any of the monitor devices would cause the switch 54 to be opened, and all information within the secured memory area 16 would be erased.